REMARKS

Claims 30, 32, 36, and 38 have been canceled. Claims 1-10, 12-14, 17, 19-23, 33-35, and 39-42 are pending. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Double Patenting Rejections

Claims (1 & 2), 3, 6, and 7 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims (47 & 48), 49, 50, and 51 of copending Application No. 11/474,495, respectively. Claims (1 & 42, 2, 4 & 5), 6, and 7 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 52, 53, and 54 of copending Application No. 11/474,495, respectively. Claims 8, 10, 13, and 19 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 43, 44, 45, and 46 of copending Application No. 11/474,495, respectively. Applicant respectfully traverses these rejections.

Pursuant to the Examiner's suggestion, a Terminal Disclaimer complying with 37 CFR § 1.321(c) is being filed to overcome the rejection. Accordingly, the rejections should be withdrawn and the claims allowed.

35 U.S.C. § 103 Rejections

Claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 7,002,823 (Ichiriu) in view of U.S. Patent 6,944,039 (Nataraj). Applicant respectfully traverses these rejections.

The Supreme Court recently held in *KSR Int'l Co. v. Teleflex Inc.* that "the [*Graham*] factors continue to define the inquiry that controls a finding of obviousness." 550 U.S. __, 82 USPQ2d 1385, 1397 (2007). The *Graham* factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459

(1966). Applicant submits that the Office Action has not properly shown that the claims would have been obvious by conducting an examination of the *Graham* factors. "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." *MPEP* 2141. Specifically, the Office Action has not explicitly or implicitly resolved the level of ordinary skill in the pertinent art.

Claims 1-7

In *KSR,* the Supreme Court stated that "[r]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at __, 82 USPQ2d at 1396. As described in the Federal Register/Vol. 72, No. 195/Wednesday, October 10, 2007 Notices, page 57534, one rationale that may be used to show that a claim would be obvious is to show some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. This is the rationale that the Office Action provides to hold that claim 1 is obvious. To reject a claim based on this rationale, however, the Office Action must resolve the *Graham* factual inquiries, which the Office Action has failed to do, and then articulate the following: "(1) a finding that there was some teaching, suggestion, or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) a finding that there was reasonable expectation of success; and (3) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness." *Id.*

In the case at hand, the Office Action has failed to make a *prima facie* case for obviousness at least because the Office Action has failed to articulate the findings necessary to maintain a finding of obviousness under the Office Action's chosen rationale. Specifically, the Office Action has at least failed to adequately articulate a finding that there was a reasonable expectation of success of combining Ichiriu with Nataraj.

The Office Action asserts that Ichiriu discloses all elements of claim 1 except "confirming proper operation of a control line used to enable output from a match line under test and the feature of enabling output from a match line under test." The Office Action states that "[o]ne of ordinary skill in the art would be motivated to combine the teachings of Ichiriu and Nataraj because the combination of Ichiriu's priority encoder & FLAG circuit and Nataraj's priority encoder/flag logic circuit comprises inputs of match signals and outputs of match addresses and match flag." *Office Action, p. 7.* The Office Action does not, however, articulate how these features of Ichiriu and Nataraj suggest "confirming proper operation of a control line," but merely lists features of Nataraj without showing a relation to the missing element.

Furthermore, the Office Action states that all but two elements of claim 1 are taught by Ichiriu, and that those not taught by Ichiriu are made obvious by being taught in Nataraj. Ichiriu, however, fails to teach six elements of claim 1, most of which are not taught by Nataraj and can therefore not be made obvious in light of Nataraj.

First, claim 1 recites "[a] method for testing a memory device comprising . . . resetting all match lines of said memory device." Neither Ichiriu nor Nataraj teach resetting all match lines. Ichiriu and Nataraj do teach precharging the match lines, *Ichiriu, col. 6, line 65; Nataraj, col. 5, lines 30-31*, the purpose of which is to bring each match line to "a high logical level at the start of a comparison operation [to then allow each line to be] pulled down to a low logical level" in the event of a mismatch. *Ichiriu, col. 6, lines 65-66.* The present specification also teaches precharging of the match lines for this purpose. *See, e.g., para. 12* ("match line remains high indicating a match"). Claim 1, however, recites resetting all match lines which, in one disclosed embodiment, means that the TM_ML_RESET signal pulses which sends a low signal to the AND gate, thus disabling the AND gate. *Para. 50.* The word line for the row being tested is then pulsed, which sends a high signal to the AND gate for the row being tested, thus enabling only the row(s) being tested. *Para. 50.* In other words, the precharging taught in Ichiriu and Nataraj is performed in the same manner in the claimed invention to bring the match lines high; however, the claimed invention then resets all of the match lines by turning off the AND gates.

While Ichiriu teaches precharging that can also bring each match line to a *low* logical level, *Ichiriu, col. 33, lines 63-65*, this is still different than the resetting of claim 1 because bringing the match lines to a *low* logical level is not what distinguishes resetting from precharging. What distinguishes resetting from precharging is that resetting occurs after precharging and is for the purpose of disabling those match lines that are not being tested. *Para. 50.* Therefore the precharging taught in Ichiriu and Nataraj is different than the resetting taught in the claimed invention. Moreover, neither Ichiriu nor Nataraj teach nor suggest resetting all match lines.

Next, claim 1 also recites as part of the method for testing a memory device, "confirming proper operation of a control line used to enable output from a match line under test." Neither Ichiriu nor Nataraj teach confirming proper operation of a control line used to enable output from a match line under test. The Office Action states that "Ichiriu does not explicitly teach the feature of confirming proper operation of a control line used to enable output from a match line under test," but claims that this limitation would be obvious to one skilled in the art in view of Nataraj. *Office Action, p. 6.* However, while Nataraj teaches a latch signal that enables a match signal to be passed to the priority encoder, *Office Action pp. 6-7*, Nataraj does not teach nor suggest confirming proper operation of any control line, including the line supplying the latch signal. As a result, modifying Ichiriu as suggested by the examiner would not be obvious to one skilled in the art because such a modification is not taught nor suggested in Nataraj.

Lastly, claim 1 also recites as part of the method for testing a memory device, "comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." Neither Ichiriu nor Nataraj teach nor suggest these limitations.

As stated in the Office Action, Ichiriu teaches a search operation comparing "the content of the memory cell with a comparand signal." *Office Action, p. 5.* Ichiriu, however, does not teach

comparing the result of the search operation with an expected result. Ichiriu teaches validity bits that record whether the data in a given row is valid. *Ichiriu, col. 7, lines 65-67, col. 8, lines 1-5.* These validity bits are used in Ichiriu to prevent matches asserted on invalid rows, *Ichiriu, col. 8, lines 18-31*, or to determine whether the result of a search operation is invalid because a match may have been asserted on an invalid row. *Ichiriu, col. 23, lines 19-25.* The validity bits, however, are not used to compare the result of the search operation with an expected result. On the contrary, a search operation involving an invalid row can still output an expected result – invalid, but expected. Ichiriu also teaches parity testing for each row, but this tests for parity during a read operation and does not test a search operation against an expected result. *Ichiriu, col. 8, lines 34-45.*

Also, Nataraj teaches methods affecting the timing of compare operations in a test mode, not comparing the result of a compare operation with an expected result. *Nataraj, col. 4, lines 42-57.* Therefore, neither Ichiriu nor Nataraj teach nor suggest comparing the result of a search operation with an expected result, confirming proper operation based on whether the result is equal to the expected result, or indicating an error if the result is not equal to the expected result.

Claims 2-7 depend from claim 1. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 8-10

The Office Action's rejection of claim 8 is similar to the rejection of claim 1. The Applicant, therefore, respectfully asserts that the rejection of claim 8 in the Office Action is deficient for the same reasons set forth above.

Claim 8 recites "[a] method of testing a memory device that includes two or more sets of memory cells and, for each set of memory cells, a match line that provides a match signal when items of data stored in said set of memory cells match a data item stored in a comparand register, the method comprising confirming proper operation of a control line used to enable output from said match line of a set of memory cells being tested." For the reasons set forth above, neither Ichiriu

nor Nataraj teach nor suggest confirming proper operation of a control line used to enable output from said match line of a set of memory cells being tested.

Claims 9-10 depend from claim 8. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 12-14

The Office Action's rejection of claim 12 is similar to the rejection of claim 1. The Applicant, therefore, respectfully asserts that the rejection of claim 12 in the Office Action is deficient for the same reasons set forth above.

Claim 12 recites "[a]n apparatus for testing a match line of a memory device, said apparatus comprising . . . a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of the match line under test based on a result of a search operation and a signal on the match line under test after confirming proper operation of a control line used to generate a signal on the word line."

First, neither Ichiriu nor Nataraj teach nor suggest a circuit coupled to a match line under test, a word line, and a test mode match line reset signal. Also, neither Ichiriu nor Nataraj teach nor suggest a test mode match line reset signal because neither Ichiriu nor Nataraj teach a signal that resets all match lines.

Next, neither Ichiriu nor Nataraj teach nor suggest "determining a status of the match line under test based on a result of a search operation and a signal on the match line under test." As stated in the Office Action, Ichiriu teaches a search operation comparing "the content of the memory cell with a comparand signal." *Office Action, p. 10.* Ichiriu, however, for the reasons set forth above, does not teach comparing the result of the search operation on the match line under test with an expected result, which would then give a status of the match line under test. Also, Nataraj teaches methods affecting the timing of compare operations in a test mode, not determining the

status of a match line based on the result of a search operation. *Nataraj, col. 4, lines 42-57.* Therefore, neither Ichiriu nor Nataraj teach nor suggest all of the limitations of claim 23.

Lastly, for the reasons set forth above, neither Ichiriu nor Nataraj teach nor suggest confirming proper operation of a control line used to generate a signal on the word line.

Claims 13-14 depend from claim 12. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 17 and 19

The Office Action's rejection of claim 17 is similar to the rejection of claim 1. The Applicant, therefore, respectfully asserts that the rejection of claim 17 in the Office Action is deficient for the same reasons set forth above.

Claim 17 recites "[a] memory circuit comprising . . . enabling circuitry that enables a match line to provide said match signal as an output when said set of memory cells is being tested, said enabling circuitry enabling the match line after confirming proper operation of a control line." For the reasons set forth above, neither Ichiriu nor Nataraj teach nor suggest confirming proper operation of a control line.

Claim 19 depends from claim 17. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 20-22

The Office Action's rejection of claim 20 refers to the rejection of claim 17. The Applicant, therefore, respectfully asserts that the rejection of claim 20 in the Office Action is deficient for the same reasons set forth in claim 17 above.

Claim 20 recites "[a] memory device comprising . . . for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said match line in

response to a signal on said word line, said enabling circuitry enabling the match line after confirming proper operation of a control line used to generate the signal on the word line." For the reasons set forth above, neither Ichiriu nor Nataraj teach nor suggest confirming proper operation of a control line used to generate the signal on the word line.

Also, claim 20 recites "[a] memory device comprising . . . control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled." Neither Ichiriu nor Nataraj teach nor suggest resetting all match lines for the reasons set forth above.

Claims 21 and 22 depend from claim 20. Accordingly, the rejection should be withdrawn and the claims allowed.

Claim 23

The Office Action's rejection of claim 23 is similar to the rejection of claim 12. The Applicant, therefore, respectfully asserts that the rejection of claim 23 in the Office Action is deficient for the same reasons set forth above.

Claim 23 recites "[a] processing system comprising . . . a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of a write enable signal used to generate a signal on the word line and determining a status of the match line under test based on a result of a search operation and a signal on the match line under test." For the reasons set forth above, neither Ichiriu nor Nataraj teach nor suggest all of the limitations of claim 23.

Accordingly, the rejection should be withdrawn and the claim allowed.

Claims 33-35

Claim 33 recites "[a]n integrated circuit comprising . . . control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled." Neither Ichiriu nor Nataraj teach nor suggest resetting all match lines for at least the reasons set forth above.

Claims 34 and 35 depend from claim 33. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 39-41

Claim 39 recites "[a] router comprising . . . control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled." Neither Ichiriu nor Nataraj teach nor suggest resetting all match lines for at least the reasons set forth above.

Claims 40 and 41 depend from claim 39. Accordingly, the rejection should be withdrawn and the claims allowed.

Claim 42

The Office Action's rejection of claim 42 refers to the rejection of claims 1 and 12. The Applicant, therefore, respectfully asserts that the rejection of claim 42 in the Office Action is deficient for the same reasons set forth in claims 1 and 12 above.

First, claim 42 recites, "[a] system comprising . . . a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for testing a match line of said CAM device, said apparatus further comprising . . . a circuit coupled to said match line under test corresponding to said word line, and a test mode match line reset signal, wherein said circuit . . . reset[s] all match lines of said memory device." Neither Ichiriu nor Nataraj teach nor suggest resetting all match lines for the reasons set forth above.

Next, claim 42 also recites "[a] system comprising . . . a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for testing a match line of said CAM device, said apparatus further comprising . . . a circuit coupled to said match line under test corresponding to said word line, and a test mode match line reset signal, wherein said circuit . . . confirm[s] proper operation of a control line used to enable output from said match line under test." For the reasons set forth above, neither Ichiriu nor Nataraj teach nor suggest confirming proper operation of a control line used to enable output from a match line under test.

Lastly, claim 42 also recites "[a] system comprising . . . a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for testing a match line of said CAM device, said apparatus further comprising . . . a circuit coupled to said match line under test corresponding to said word line, and a test mode match line reset signal, wherein said circuit . . . [1] compar[es] said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; [2] confirm[s] proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and [3] indicat[es] an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.." For the reasons set forth for claim 1, neither Ichiriu nor Nataraj teach nor suggest these limitations.

Accordingly, the rejection should be withdrawn and the claim allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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